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No. 4 ESS:

Peripheral System

By J. H. HUTTENHOFF, J. JANIK, JR., G. D. JOHNSON, W. R. SCHLEICHER, M. F. SLANA, and F. H. TENDICK, JR.

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The No. 4 ESS peripheral system economically performs essential switching and signaling functions. A modern time-division switching network has been developed to meet rapidly growing traffic demands and provide a basis for the all-electronic telecommunications network of the future. Common-channel interoffice signaling (CCIS) provides high-speed interprocessor communication via data link. Signal processor units perform routine signaling tasks such as scanning and digit collection, effectively increasing the main processor's capacity. To a greater degree than in previous systems, the vital man-machine interfaces are enhanced with sophisticated interactive capability.

I. INTRODUCTION

Electronic switching systems, in modern terminology, are composed of two parts, the central processing unit and the peripheral system. In No. 4 ESS, the central processing function is performed by a new high-speed integrated circuit unit, the 1A Processor, described in a special issue of the B.S.T.J.[1] The essential interconnection, signaling and interface functions of the No. 4 ESS peripheral system are the subject of this paper.

The switching network developed for No. 4 ESS features a new PCM time-division architecture that effectively integrates modern switching and transmission technologies. Interoffice trunks are handled via a multiplexed format, with no need to derive individual channels, and with no need for much of the per-channel equipment required in previous toll switching machines. Significant economies in administration and maintenance also result from this configuration. The multistage time-space-time topology chosen enables a large, high-traffic-occupancy

switching network to be constructed, as required in large metropolitan area switching centers. The planning, design, and operation of this new switching network is detailed in Section II.

Several special interoffice signaling equipment units have been developed for No. 4 ESS. These recognize and process information that identifies the address or destination of a call or any change of status of the call. A new Common Channel Interoffice Signaling (CCIS) unit is being introduced, permitting direct intercommunication via a data link between modern stored-program controlled switching offices. In addition, two new signal processor units, SP1 and SP2, are being provided with No. 4 ESS to relieve the 1A Processor of many repetitive time-consuming tasks such as counting dial pulses, timing critical intervals, or assembling several multifrequency signaling digits for presentation to subsequent address-determining programs. SP1 is designed with a multiplicity of scan and signal distributor points for sensing and controlling up to 4080 analog trunks. SP2 is designed to interface effectively with the bit-stream signaling used in digital carrier systems. A description of these signaling interfaces is given in Section III.

Section IV explains the bus system used to exchange orders and information between the 1A Processor and the multiplicity of peripheral equipment units.

Much effort went into the planning and development of the man/machine interface facilities provided in No. 4 ESS. Specialized operating and maintenance centers located outside the equipment rooms are equipped with sit-down consoles and with interactive Cathode-Ray Tube (CRT) displays having access to very large information data bases. These man/machine interface features are outlined in Section V.

Development of No. 4 ESS could not have occurred without the almost concurrent development of a family of highly reliable, microscopic-size, silicon integrated circuits, which permitted the design of new switching frames with over 100,000 logic gates. Section VI covers the equipment design philosophy used in No. 4 ESS.

The following sections of this paper provide a more detailed explanation of the No. 4 ESS peripheral system.

II. SWITCHING NETWORK

2.1 Principal characteristics

The switching network is the center of interest in the overall planning and design of a new toll electronic switching system, and has important operational and economic influences on the future of the long-distance telephone business.

Long-distance telephone usage is expected to increase about 150 percent in 10 years, and to continue this trend into the '90s. Much of this

increased usage will originate in large metropolitan centers. This rapidly growing, concentrated traffic demands a new high-capacity toll switching system with a switching network much larger than present units.

Conventional space-division switching networks tend to become less efficient and more expensive as their size increases. The goal of No. 4 ESS is to be cost-competitive with existing systems while also meeting the large size requirement. This goal clearly indicated the need for a nonconventional approach to the design of a new toll switching network.

Only after several years of study and planning was the development of the final network begun. Starting in 1968, Bell Laboratories conducted an extensive evaluation of several network types that appeared to be suitable for modern message switching service. Space-division networks employing sealed metallic crosspoints such as the ferreed were studied, as well as those with solid-state PNPN crosspoints. Delta modulation was considered as a means to overcome the variable attenuation of the solid-state crosspoints. Time-division networks were extensively evaluated, especially PCM digital hybrid types employing time switching and single- and multiple-stage space switching configurations. Logic designs and feasibility models were completed and cost estimates were made.

The various network types were compared according to the following criteria:

(*i*) The network should be at least three times larger than that of the present 4A crossbar system.

(*ii*) The network should be substantially nonblocking to eliminate load-balancing and minimize administrative effort.

(*iii*) The network should function efficiently in the rapidly growing digital transmission environment, as well as with conventional analog facilities.

(*iv*) The network must be cost-effective, both in terms of first cost and in terms of annual charges for maintenance and administration.

(*v*) The network must operate harmoniously and efficiently with the stored program processor.

As a result of this extensive evaluation and other system studies, the hybrid time-space-time network shown in Fig. 1 was selected for use in No. 4 ESS.

This network was chosen because:

(*i*) It satisfies all requirements.

(*ii*) Transmission plant is moving toward increased use of digital facilities.

(*iii*) Installation effort and floor space are reduced.

Fig. 1—No. 4 ESS network.

(*iv*) The digital interface leads to future cost reductions in terminal equipment.

The time-switching functions take place in time-slot interchange (TSI) units and the space-division switching functions take place in time-multiplexed-switch (TMS) units. A full-size network comprising 64 TSI and 8 TMS frames can handle over 107,000 four-wire trunks and service circuits. This is a folded, single-sided configuration where any network port can be connected to any incoming, outgoing, or two-way trunk. No double connections are required for two-way trunks.

The 1A Processor resident software controls the network as shown in Fig. 2. This software has the responsibility for path selection, for path setup and takedown, and for administering the map which lists the busy-idle states of all time slots and network links.

The network contains independent memory units which, by repetitively cycling 128 times per PCM frame interval, maintain all speech paths once they are set up by the processor. These network memories duplicate the path linkages contained in the processor's map. Network connections are maintained autonomously, even with momentary processor outages. The hardware-software interface and the path selection process were carefully designed to minimize processor usage.

A network traffic simulator was developed to determine the effect of various path-hunt algorithms on network blocking and to determine the processor efficiency in selecting paths. The simulator modeled a full-size network. Shown in Fig. 3 are the results of the simulation. The figure

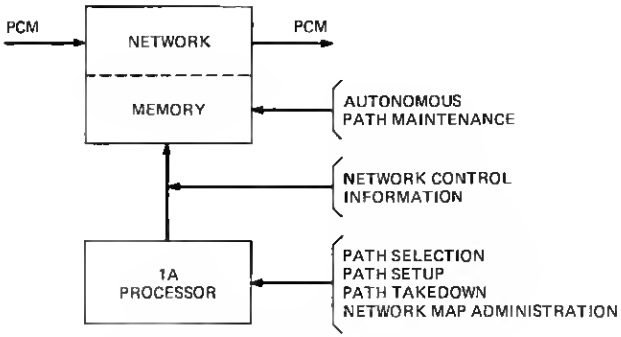

Fig. 2—No. 4 ESS network control.

of timing pulses, which are distributed to the TMS and TSI frames and through their clocking circuits to the transmission and toll terminal equipment for further use. In addition, the network clock frame contains a system clock unit providing timing signals readable by software in the 1A Processor, as well as time-of-day at the master control console.

The network clock (NCLK) contains four 16.384-MHz quartz crystal oscillators, each having a long-term stability of 1 part in 10 billion per day and a lifetime stability of 1.6 parts in 100 million. The oscillators normally run in a mode wherein one oscillator is designated as master, with the remaining three oscillators operating in the slave mode, phase locked to the master oscillator. Although normally arranged in an established hierarchy with the 00 clock chain oscillator designated as the master, any oscillator can be master and the clock can operate with as little as one good oscillator. The master oscillator selects control, and the monitor circuit in each chain automatically determines from error inputs whether its associated oscillator is healthy or defective, and thus determines whether the oscillator in chain 00 should be switched to chain 01, 10, or 11. In general, the highest healthy oscillator in the hierarchy is selected as master to the other oscillators, which are then phase-locked to it.

The phase-lock circuits detect and interpret phase and signal-level errors to ensure that the oscillator output is within ±5 degrees deviation of the master. Pulse-shaping and frame-pulse generation circuits serve to combine the 16.384-MHz signal from one clock chain with that of the other clock chain in the bay, and shape the resultant signal into a symmetrical square wave. In addition, a counter in the frame pulse generation circuit counts the pulses and generates a signal every $\frac{1}{8000}$ second to eliminate the 2048th pulse from the outgoing pulse train, thus defining the 8-KHz PCM frame pulse to the TMS and TSI. The clock cable drivers distribute the duplicated clock signal to TSI and TMS units over predetermined lengths of coaxial cable.

2.3.2 Time-multiplexed switch frames

The TMS frame (Fig. 6) is organized as a simplex two-stage 256 × 256 switch array, with each stage composed of 16 × 16 arrays of crosspoint logic gates. Each TMS is contained in a 7-foot high, 4-foot 4-inch wide two-bay frame and consists of two peripheral bus units, a controller and bus interface unit, a control unit, eight-switch units, and miscellaneous power and filter units.

The TMS frame provides no duplication of switches within the frame. Each TMS frame has a mate frame which performs the same switching function. If either frame should fail, its mate performs the switching function without loss of calls. There may be one, two, or four pairs of

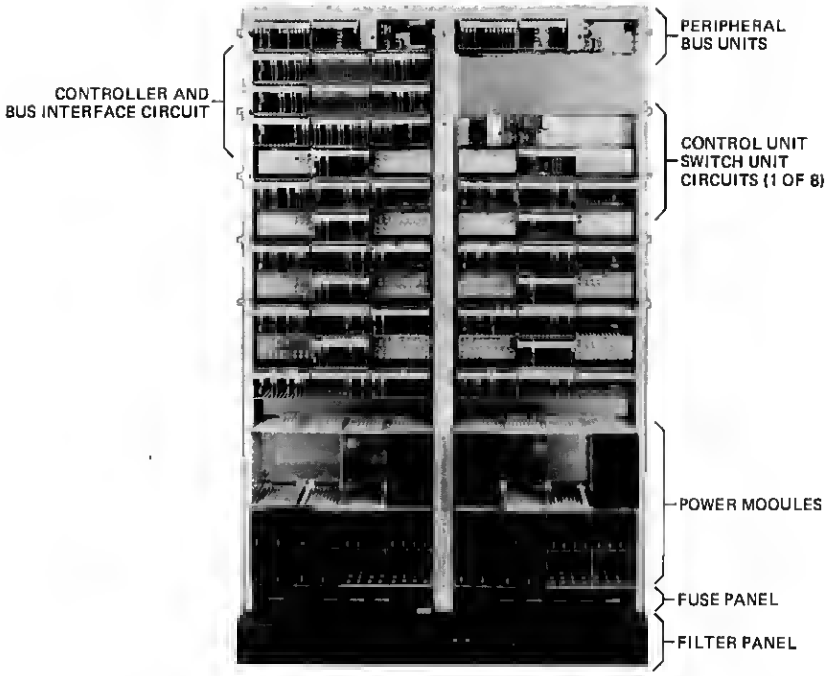

Fig. 6—Time-multiplexed switch frame.

mated TMS frames in a No. 4 ESS office. Moreover, circuit packs may be added to the switch units in four discrete steps so that the individual frames can grow in capacity.

In a full size No. 4 ESS office, four pairs of TMS frames are provided in a duplicated two-stage 1024 input by 1024 output switch array, providing 1024 unidirectional paths between input and output in each time slot. Each connection is capable of providing a path for an 8-bit PCM sample of data (representing a voiceband signal) in each time-slot. Each network connection through the TMS frames is made in terms of a pair of unidirectional paths in one of the 128 time slots, sharing the paths on a repeating basis at an 8-kHz rate. A total of 135,000 network paths (1024 × 128) are possible in a four-TMS-pair office, with each path being set up cyclically 8000 times per second.

The PCM samples arrive as part of a pulse train from the TSI frame over coaxial cables, where the samples from any one conversation, arriving once every 125 μsec, are interleaved in 128 time slots with the samples from other conversations, and enter the switch units where cable receivers reconstitute the signals and translate them to 1A logic levels. The signals are then passed through the appropriate crosspoint gates in the two stages of TMS switching, and are presented to coaxial cable

drivers where they are amplified and transmitted to the other TSI frames over coaxial cables.

The switches are controlled by information contained in time-slot memories. The information for the connections is placed in these memories by the call-processing programs, which (via instructions over the peripheral unit buses) direct the frames to set up the paths connecting the incoming and outgoing calls. This path information is decoded in the controller, which then inserts the connection information into the time-slot memories where it is read out to provide a path through the network in a given time slot. The memories are accessed from the controller for a directed read or write for call-handling purposes in one half of each time slot, and are read in the second half of each time slot, under control of a counter synchronized to the network clock, to provide the path information for the next time slot.

The TMS does no retiming of the PCM data; rather, the TMS simply closes the data path and allows the data to pass through. This requires precise control of delay, which is provided by accurately cut coaxial cables between TSI and TMS frames and between NCLK and TSI/TMS frames.

The duplication existing between the paired TMS frames is further accounted for by a matching interface, provided between mated pairs of TMS frames in order to verify that the two frames are operating in step and also to further verify that the frames are operating properly. A mismatch of control data between the two frames causes an error indicator to be set in the frame detecting the mismatch.

2.3.3 Time-slot interchange frames

The Time-Slot Interchange (TSI) frames provide the initial time-space (T-S) and final space-time (S-T) switching stages of the No. 4 ESS time-division network. The TSI frames accept incoming PCM samples from the analog and digital facilities (voiceband interface frames and digroup terminals) over coaxial cables which carry the signals in a DS-120 format, wherein 120 8-bit PCM channels are time-multiplexed in a 128 time-slot, 16-bit per time slot, 16.384-MHz channel. The eight time slots not used for PCM channels are used for maintenance functions. A TSI frame interfaces with 14 DS-120 links, and thus is capable of handling 1680 trunks.

The receiving portion of the TSI buffers the incoming DS-120 links to allow synchronization of the incoming data with the network timing, then decodes and decorrelates the data, and performs the initial T-S switching prior to transmitting the data samples to the TMS frame.

After passing through the TMS frame, the data return to the transmitting portion of the same or another TSI, where the final S-T switching is performed on the data. After passing through these stages, the

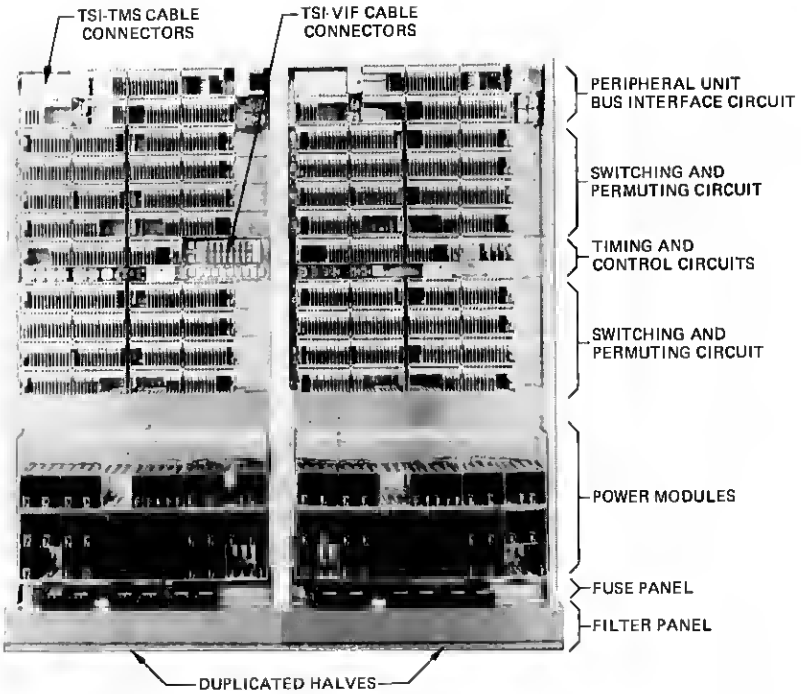

Fig. 7—Time-slot interchange frame.

transmitting portion of the TSI then recorrelates and reloads the data into outgoing DS-120 links, where the data are then transmitted to the appropriate analog and digital facilities.

The TSI frame is a 7-foot-high, 6-foot 6-inch wide frame, which contains duplicated peripheral hus interface units, duplicated timing and control units, two duplicated switching and permuting circuits, and power and miscellaneous units (Fig. 7).

The TSI frame is controlled hy programs stored in the 1A Processor; the peripheral unit hus provides the means hy which the 1A Processor accesses and controls the TSI. Thus, the peripheral hus interface unit sends information to, and receives information from, the peripheral unit hus system, and gives these instructions to and receives timing from, the timing and control unit.

The timing and control unit performs a numher of important functions which control and sequence the operation of the TSI frame, and particularly the switching and permuting circuits. The timing and control unit receives a 16.384 MHz signal from the network clock frame, and uses this signal to drive a counter whose phases are decoded to provide timing and addressing for all autonomous operations performed within the TSI

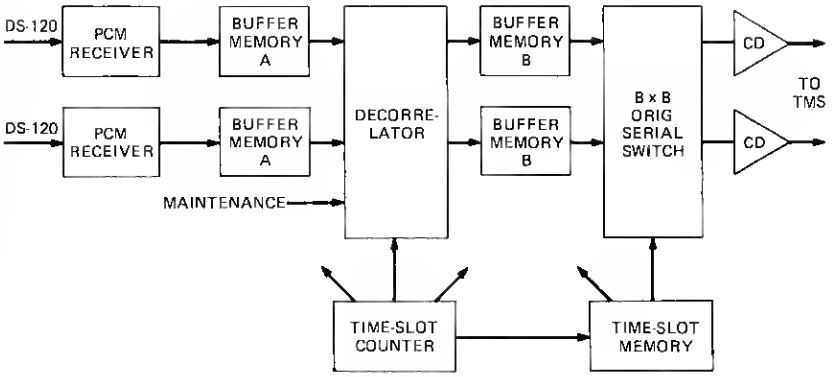

Fig. 8—Switching and permuting circuit (receive).

frame. In addition, the 16.384 MHz clock is also converted to an 8.192 MHz signal and transmitted, via a DS-120 link, to the transmission facilities connected to that TSI frame. The timing and control unit also provides decoding and sequencing for control and maintenance orders received via the peripheral unit bus, and records occurrences of autonomous errors detected in the frame for subsequent maintenance and diagnostic purposes. In addition, the unit provides control access (read/write) to the time-slot memories and busy/idle map memories in the switching and permuting circuits. Finally, matching of data between the duplicated timing and control units is provided to perform a vital diagnostic capability within the TSI frame.

Data arrive at the receive side of the switching and permuting circuit (Fig. 8), via the serial DS-120 link. This terminates on the PCM receiver, where the data (8-bit PCM) samples are converted to a 9-bit parallel form by addition of a parity bit, and placed in a first buffer memory (buffer memory A), at the address determined by the word count of the incoming PCM data. This provides a retiming function which allows independent operation of the transmission facility and the switching network. The reading of buffer memory A, as with all subsequent functions performed on the data in the TSI frame, is under the control of the time-slot counter in the frame.

The next operation is the performance of the deloading and decorrelation of the incoming data streams. For this operation, the data are read from buffer memory A in synchronism, transferred across the decorrelator in parallel format, and written into buffer memory B. The location from which the data are read from buffer memory A, and the location into which the data are written into buffer memory B is the count of the time-slot counter—i.e., at time slot x, words are read from buffer memory A location x and written into buffer memory B location x. The decorrelator may be thought of as an 8×8 switch with a fixed algorithm wiring

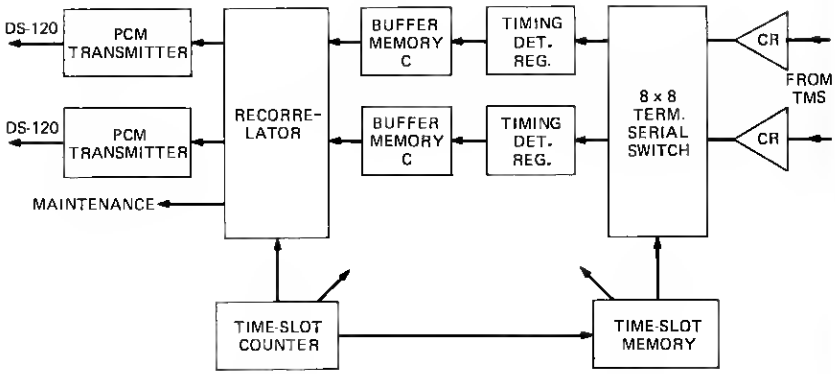

Fig. 9—Switching and permuting circuit (transmit).

pattern. Seven DS-120 links terminate on each switching and permuting circuit. The eighth input to the decorrelator is used only for maintenance and diagnostic purposes. Eight outputs from the decorrelator are available for access to eight buffer memory B's.

Operationally, the decorrelator spreads the traffic incoming on each DS-120 link equally over the eight buffer memory B's, so that each buffer memory B will store one-eighth of the samples from each input. Since there are seven inputs, each with 120 trunks, each buffer memory B will contain the samples from seven-eighths of 120, or 105 trunks, and will contain only 15 trunks from each DS-120 input. This deloads the network input and minimizes any effects of correlation of trunk seizure and holding times such as might occur with a large trunk group (perhaps as large as 120 trunks) arriving on a single DS-120 link.

When it is determined that a new network connection is to be established, call-processing programs resident in the 1A Processor are entered which search for an appropriate idle path through the network. Information specifying the time slot to be dedicated to the new connection, as well as the space switch linkages, is sent to the TSI via the peripheral bus interface. Through the control unit, this information is interpreted and stored in the time-slot memory. As the time-slot counter advances, the contents of the time-slot memory are read out, one cell at a time. A group of these bits defines the address of the buffer memory B to be read in that particular time slot, thus time-switching the incoming PCM channel information. A second group of bits provides the information needed to control the 8 × 8 space switch that directs the PCM word from buffer memory B to the TMS frame.

The PCM signal generally returns from the TMS to the transmit side of a different switching and permuting circuit from one in which it originated. As shown in Fig. 9, the signal is passed through the fourth stage of space switching—an 8 × 8 time-shared switch—then through

a timing detector and register where moderate amounts of time slips between paths are accounted for, and into buffer memory C, where the second stage of time-switching is performed. A corresponding time-slot memory associated with buffer memory C contains the data which selects the path through the 8 × 8 switch and the information for the time switch in a manner analogous to that discussed previously.

The block diagram (Fig. 9) shows the transmit portion of the switching and permuting circuit. After the data are stored in buffer memory C, the data are read out synchronously by the time-slot counter, passed through a recorrelation switch which performs an inverse mapping of the decorrelation function, and sent, via a transmitter (which conditions the signal into a DS-120 format), to the transmission facilities, voiceband interface frame or digroup terminal.

III. SIGNALING INTERFACES

3.1 Overview

Interoffice signaling is the information that identifies the address or destination of a particular call or change of status of a call. In No. 4 ESS, this signaling is monitored and controlled via the signal processors and CCIS terminal groups which are, in turn, controlled by the 1A Processor via the peripheral unit bus. There are two types of signal processor frames: Signal Processor 1 (SP1) which can handle signaling for up to 4080 analog trunks, and Signal Processor 2 (SP2), which can handle signaling for up to 3840 digital trunks. The signal processors can process both Dial Pulse (DP) and Multi Frequency (MF) signaling formats. Each CCIS terminal group frame can process common channel interoffice signaling for up to 24,000 trunks.

Much of the work done by a switching system in processing calls is associated with supervisory scanning and with the collection and transmission of the address digits. In No. 4 ESS, the signal processors and CCIS terminal groups autonomously execute these repetitive and time-consuming data processing functions performed by the central control in previous electronic switching systems. This eliminates the overhead that would exist if the data processing functions were done by program control in the 1A Processor, allowing a higher call-handling capacity. Call-processing programs resident in the 1A Processor maintain control over the overall handling of a call. Decisions as to how many digits are to be collected on MP or DP calls, what action to take on seizure or disconnect, etc., are determined there.

The CCIS signaling equipment for No. 4 ESS will be described in a later special B.S.T.J. issue on CCIS and will not be described in detail here. The signal processors will be presented by first giving a detailed description of the SP1 design. Since many parts of the SP2 design are

identical to SP1, the SP2 will then be presented by describing only those parts which are different from SP1.

3.2 Signal Processor 1

3.2.1 Description of Signal Processor 1

The SP1 is a duplicated, wired-logic processor which performs the various scan, distributing, and digit-reception tasks for analog trunk facilities. Furthermore, it is a directed processor under control of CC. In order to execute these tasks, the SP1 control interfaces internal matrix-access circuits and communicates with CC via the peripheral unit bus. Each SP1 has 4096 simplex scan and 4096 simplex distributor points for control of up to 4080 trunks. These are designated universal scan and distributor points and connect to the E and M leads, respectively, of the trunks in the Unitized Terminal Equipment (UTE) facilities and miscellaneous trunk frames. A scan point and distributor point are assigned to each trunk.

In addition 2048 scan and distributor points, designated miscellaneous points, are used for control of service circuits and miscellaneous circuits and alarms. Included in this category are MF transmitters and receivers. MF signaling equipment is not assigned to a single trunk but is instead shared by many trunks on an "as needed" basis. No. 4 ESS uses a new integrated circuit MF receiver and transmitter. Trunks requiring MF receivers or transmitters are connected to these units through the switching network for the time required to receive or transmit a call and they are then released for use by other trunks. Up to half of the miscellaneous distributor points can be pulse points, transformer coupled to supply 500-ns control pulses for peripheral control functions. All scan and signal distributor points provide dc isolation to prevent ground loops.

The SP1 interfaces with new and existing signaling equipment through its scan and distributor points. Autonomously every 10 ms the SP1 scans all 6144 scan points, stores changes of status and digits received in internal buffers, and performs nearly all timing functions on MF and DP reception and transmission. Upon command the SP1 also executes directed orders from the 1A Processor to empty the internal buffers containing collected digits, seizure reports, and disconnect reports, and to operate distributor points or read groups of 16 scan points. CC also can load internal work lists with digits to be transmitted to other offices. Once loaded, the digits are transmitted autonomously by the SP1.

In addition to handling signaling in a No. 4 ESS office, the SP1 monitors and controls miscellaneous circuits in an office such as alarm circuits and power switches. This provides the interface that allows CC to control the entire periphery. Two signal processors in each No. 4 ESS office are

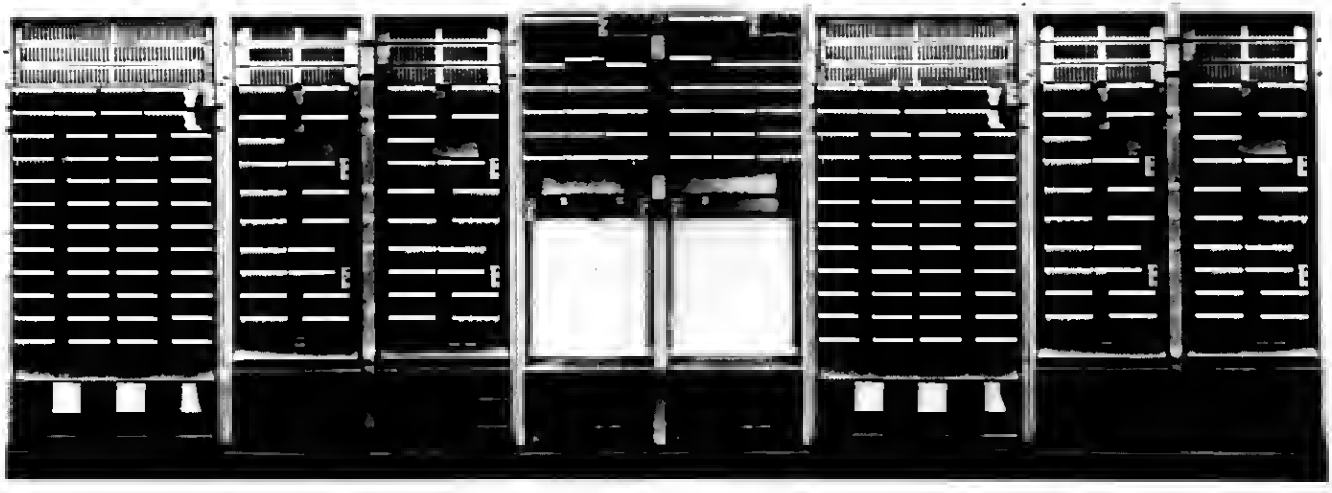

Fig. 10—No. 4 ESS signal processor.

designated as base SPs; they are initialized via CC pulse points. The base SPs in turn supply duplicated pulse points to initialize or "bootstrap" the remainder of the periphery on a per frame basis.

A photograph of the SP1 frame appears in Fig. 10. The right-hand matrix and applique are optional, and, within each matrix frame, growth is provided by groups of circuit packs for 1024 points. The matrix frames will be described first, and will be followed by the control units. The matrix frames provide the actual interface with the equipment to be controlled or monitored, while the control unit provides the actual data storage and processing.

3.2.2 Distributor and scanner matrix

The distributor and scanner matrix frames are simplex units accessed by a duplicated control unit via duplicated access circuits. The access accepts a 9-bit address and reads out a row of 16 points. The distributor access contains additional circuitry so that a row of 16 flip-flops, storing the status of 16 distributor points, is selected and may be individually set or reset. The interface of the matrix with the duplicated access is an AND function so that only when the access circuits from both controllers agree is a row selected. A successful selection generates an ALL SEEMS WELL output. An ALL ZEROS TEST checks for stuck conditions, especially a stuck ALL SEEMS WELL. This prevents access-circuit faults from causing service disruptions.

3.2.3 Signal Processor 1 control

The functions of the control can be divided into two classes—directed and autonomous. A directed function is the result of a PU bus order from CC and immediately results in some action and/or a response back to CC. Directed functions, for example, would include reading an output buffer, reading the present state of 16 scan or distributor points, writing up to 16 distribute points, and reading or writing data or a control memory word.

Autonomous functions are the repetitive and time-consuming functions performed by the SP1 that remove the heavy burden from CC. These functions are performed on a 10-ms cycle as shown below.

The 10-ms base-level cycle (Fig. 11) was selected to meet the timing precision of MF and DP outpulsing and still allow the SP1 to process a reasonable number of scan points each cycle. The first half of each cycle is devoted to MF outpulsing, universal scan, and DP digit reception, while the second half is devoted to MF outpulsing, miscellaneous scan, MF reception, and DP outpulsing. Note that MF timing must be performed every 5 ms or twice each cycle to meet both domestic and international signaling requirements.

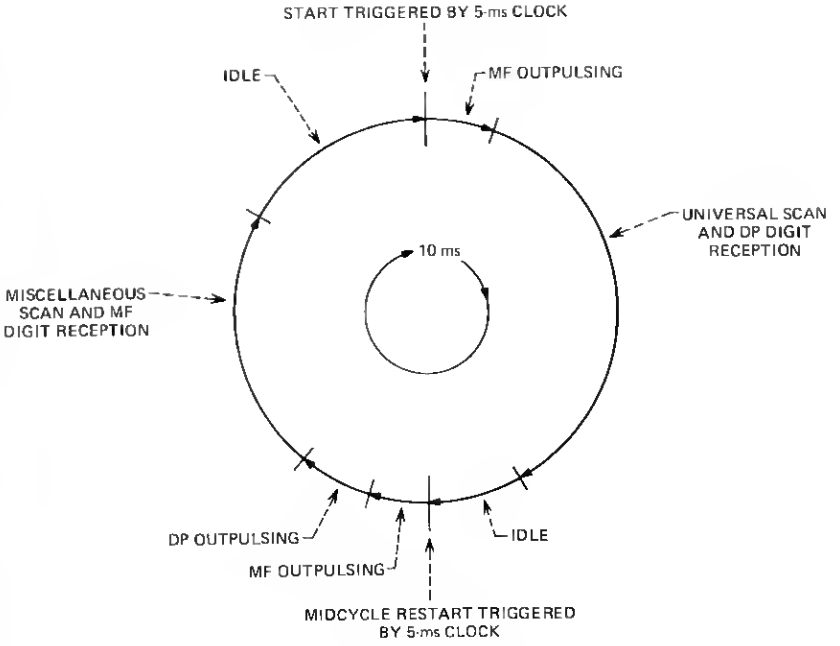

Fig. 11—SP base-level timing.

Figure 12 is a block diagram of the SP1 control, whose organization is similar to that of a stored program processor. There is a bus structure that provides access through the control unit for all the various subunits. The autonomous sequencers are the heart of the control. An executive sequencer is the highest-order sequencer and activates three autonomous task sequencers in the order and frequency specified by the 10-ms base cycle. It also performs sanity checks to ensure that each task has been

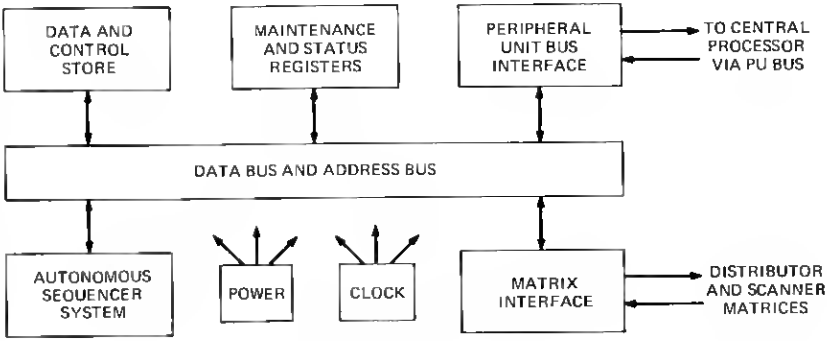

Fig. 12—Signal processor control.

completed the correct number of times. The scan and digit reception sequencer, one of the three task sequencers, performs both the universal and miscellaneous scan tasks and in addition performs both MF and DP reception. The other two task sequencers are the DP outpulsing sequencer and the MF outpulsing sequencer. Each task sequencer, when called, performs its task for all associated elements and returns control to the executive sequencer upon completion. The three task sequencers in turn may call in the matrix sequencer or memory sequencers which return control to the calling task sequencer upon completion.

The peripheral unit bus interface contains the cable drivers and receivers which interface the parallel data PU bus to the SP1 control. It listens for PU bus orders destined for the SP1 and carries them out on an interrupt basis. An internal clock supplies appropriate timing pulses. A countdown circuit provides synchronized 5-ms, 10-ms, and longer outputs for various purposes such as interdigital timing.

3.2.4 Data and control store

The data and control store is used by each of the autonomous task sequencers for storage and retrieval of processing data, for storage of processing instructions from CC and for buffering reports to CC. The store logic structure is conventional except for insertion masking and address increment logic. Also, counters are used to keep addresses (pointers) for list entry points.

The store contains four buffers of varying lengths: the seizure, digit, high-priority and low-priority buffers. They store autonomously collected information destined to be sent to CC. Each buffer is a first-in, first-out list. The type of information put in each is indicated by its name, with the high-priority buffer generally containing answer and disconnect signals. The CC interrogates these buffers periodically and requests the information. The store also contains work lists used by the autonomous sequencers for DP and MF reception and outpulsing.

3.2.5 Trunk status bits

Information for each trunk assigned to an SP1 is contained in its trunk status bits. The trunk status bits occupy three-quarters of the store and control the scan and digit reception sequencer on a per-trunk basis. Six bits of each word are permanently assigned to each of the scan points in the scan matrix. These bits are designated T1 through T6. The bits for four trunks are stored in one memory word. T1 is the state of the scan point at the last time the SP1 scanned the point. Thus the SP1 can recognize and report a change of state. T2 and T3 tell the SP1 what to do if there is a change of state. These bits are set by CC via a PU bus order. The report code specifies whether the SP is to ignore the change of state

or report changes in a buffer. For example, if the scan point is in the universal field and the change of state is to off-hook, the report will be put in the seizure buffer instead of the low-priority buffer. If the digit buffer is specified, the SP1 will create an entry on the dial-pulse reception work list and begin to report digits rather than individual state changes for that trunk.

T4 and T5 are used for hit timing if T6 has been set by CC. If the change of state persists for 30 to 40 ms, the change of state will be reported. This feature is used primarily to protect against false seizures.

A block of eight words is reserved for SP1 maintenance programs. Specific patterns are stored in these words at the time a unit is placed in service. Whenever an interrupt occurs, the words are accessed to provide a quick check of peripheral-access, internal-bus, and memory-access circuitry.

3.2.6 Maintenance and status registers

Four register groups provide the means for controlling SP1 controller configuration and service status, recording failure information and reporting errors to the CC, and forcing special maintenance circuits which enable CC programs such as SP diagnostics to detect and resolve circuit faults. Error detection and maintenance circuitry is distributed throughout the SP1. The error-source register records the source of an error discovered by these circuits. The hardware checks in the simplex category are parity failure of store information, invalid sequencer states, DP work lists out of order, etc. Duplex checks are primarily matches between registers and sequencers of the duplicated control.

The action on detection of an error is to record the error and stop. At regular intervals, CC polls all units to locate any unit in trouble. Fault recognition programs then determine the faulty unit. Read and write access plus clock control via PU bus maintenance orders permit quick checks hy fault-recognition programs, and intensive, accurate error location by maintenance programs.

3.3 Signal Processor 2

3.3.1 Description of Signal Processor 2

Each Signal Processor 2 (SP2) monitors and controls signaling for a total of 3840 digital trunks via four digroup terminals.[2] The SP2 performs data processing functions—scanning, digit reception and outpulsing, etc.—and interacts with the 1A Processor in the same manner as the SP1. Hence, the SP2 is similar to the SP1 with two principal exceptions. First, instead of physical scan and distributor point circuits for the universal points, the supervisory state of each trunk is stored as a bit in 512 words

of additional memory. Whenever the autonomous data processing functions need to read or write universal supervisory states, the SP2 matrix sequencer accesses the data memory. Second, the SP2 acts as the communication link to provide, in effect, an extension of the peripheral unit bus to the digroup terminals for maintenance and control messages.

3.3.2 Supervisory data transfer and timing

The incoming supervisory state of each trunk is extracted from the T-carrier line facility by the digroup terminal (DT). Upon request by the SP2, the data is sent to the SP2 on a serial data link to be stored in the SP2 data memory. Similarly, and simultaneously, outgoing supervisory data is sent from the SP2 to the DT to be injected into the outgoing T-carrier data stream. The timing of the data transfer is such that the average delay is less than 3 ms, which means that the overall delay with the SP2 is less than with the SP1 because there is essentially no delay in the DT compared to relay operate delay in the metallic trunks and the delay of single frequency sets on the analog trunks associated with an SP1.

3.3.3 DT control and maintenance messages

The SP2 acts as a communication link between the DTs and the peripheral unit bus. Program commands for a DT from the 1A Processor, such as protection switch or error source readout requests, are sent on the peripheral unit bus to the SP2 and temporarily stored in memory. At the start of data transfer to the intended DT, the SP2 first transmits the message and then starts the data transfer. Similarily, a message from the DT is transmitted to the SP2 and placed temporarily in memory.

When signaling for digital trunks is via CCIS, the DT acts as a transmission multiplex and terminal without supervisory signaling. For this situation the SP2 acts as a control and maintenance message link to the peripheral unit bus for up to 12 additional DTs.

3.3.4 Error detection and redundancy

The DT and the SP2 contain error-detection and configuration circuits and both have duplicated control circuits. Normally DT controller zero is configured to SP2 controller zero and similarily with controller one. In this mode there is continuous matching in the SP2 of all information and sequencer action. In the event of a fault, either DT controller can be configured, by peripheral unit bus messages to the SP2, to either half or both halves of the SP2.

3.3.5 Supplementary matrix

In a largely digital office there still exists a need for miscellaneous physical scan and distribute points for such functions as recognition of

fuse alarms and for controlling multifrequency transmitters and receivers. A supplementary matrix frame is available as an option for the SP2. The supplementary matrix contains 1024 scan and 1024 distribute points arranged to correspond directly with the first 1024-point miscellaneous matrix of the SP1 scan and distribute matrix.

IV. PERIPHERAL UNIT BUS SYSTEM

The peripheral unit bus provides the control and data path between the 1A Processor and most peripheral frames of the No. 4 ESS. The bus consists of four duplicated bus groups: the enable address bus, the write bus, the reply bus, and the control bus. The enable address and the write buses convey instructions and information in parallel form from CC to the peripheral units, while data is sent from a peripheral unit to CC via the reply bus, also in parallel form. Control and maintenance information is transmitted to and from the peripheral units over the control bus.

Because of the limitations of the length of the bus and the numbers of frames that could be connected to a single bus, a Peripheral Unit Bus Branching (PUBB) frame is provided to extend the peripheral unit bus. The PUBB is a fully duplicated frame, with separate units for PU bus 0 and PU bus 1. It is growable to four units per bus with four bus branches per unit. Loop-around circuitry in each unit allows fault-recovery programs to check the integrity of each branch up to the output of the PUBB frame. Since all signals entering the PUBB are regenerated internally and transformer-coupled to the outputs, the PUBB also provides isolation of the periphery from the 1A Processor.

Outgoing signals pass through serial bus receivers in the peripheral units being serviced. Bypass resistors on the receiver circuit pack connectors assure bus continuity when a receiver pack is removed for repair. Shunt cable drivers in each peripheral unit send data back to CC. The last peripheral unit on a bus branch contains terminating resistors to preserve the transmission characteristics of the bus. Because all connections to the bus are transformer coupled, the bus provides complete ground potential isolation between units. Care is taken in engineering an office to assure that critical frames do not all appear on the same bus branch.

All No. 4 ESS peripheral units are alerted via coded enabling, whereby each unit has a unique name and listens to the bus at all times. When an order is sent over the peripheral bus, only the peripheral unit whose name matches the name accompanying the order will respond.

V. MAN/MACHINE INTERFACES

The craftsperson has several facilities with which to interface No. 4 ESS. The major facilities are the Master Control Console (MCC), the

Fig. 13—Master control console.

DATASPEED® 40 terminals, the power control switches located on the peripheral units, and the office alarm system.

The Master Control Console (Fig. 13) is located in the Maintenance Operations Center (MOC) and consists of an alarm, control, and display console that serves as a direct communications link between the craftsperson and the system. It indicates by means of alarms and status indicators the current condition of the system. Controls are provided so that manual recovery of the system can be effected if the automatic recovery capability is unable to do so. The displays and controls have been designed to be as simple as possible and care has been taken to avoid any arrangement of controls and displays that might mislead or confuse the craftsperson. An equipment status panel on the MOC provides the craftsperson with the overall status of the system. Any unit out-of-service for any reason, including diagnostics, will activate an indicator lamp for that unit type. By depressing the key associated with the indicator, the craftsperson is furnished with a printout of the member numbers of all units of that type which are out-of-service.

The *DATASPEED* 40 terminal is the major man/machine interface between the craftsperson and the peripheral units. From the terminal it is possible to remove a unit from service, diagnose it, and restore it to service. This can be done via several I/O channels located throughout the No. 4 ESS office. The primary terminals used are those located in the MOC area. In addition, two beltline I/O channels are distributed to all peripheral units so that the craftsperson can interface with the system at the frame being repaired. Messages to and from the craftsperson are simple and concise. In the case of a circuit-pack replacement, the pack

type and frame location identified by diagnostics are given to the craftsperson.

The craftsperson also has limited control over a peripheral unit with the power control switches located on the peripheral units. Operation of the switches requests removal of a frame from service. An indicator lamp on the switch shows whether the request is being serviced and the state of the frame (out-of-service). Similarly, it is possible also to request restoral of a peripheral unit to service, which will automatically cause diagnostics to be run on the unit. If the unit passes diagnostics and is restored to service, all indicator lamps will be extinguished. Finally, manual power alarm tests on the unit power converters can be performed from the power control switch.

The craftsperson is alerted to failures in the system by the No. 4 ESS office alarm system. This newly designed system consists of a series of alarm grids, each monitoring a specific area of the periphery. Alarm outputs, both audio and visual, can be limited to only the area being monitored and its associated work center or can also be directed to other areas or work centers via software controls. Grids can also be joined into larger grids via software to accommodate a reduced work force at non-peak hours. The status of all grids is displayed in the MOC. Audible alarm outputs are included to indicate software alarms as well as hardware or power alarms.

VI. EQUIPMENT DESIGN

Development of the No. 4 ESS peripheral equipment would not have been possible without dramatic advances in miniaturization of electronic circuitry. This rapid advance was based upon the development of Silicon Integrated Circuit (SIC) technology. The fact that a minute SIC chip may contain as much or more circuitry than was previously contained in an entire plug-in circuit pack has had a tremendous impact on the development of No. 4 ESS equipment, permitting the design of frames which contain over 100,000 electronic gates.

In order to produce the 1A Processor, with high-speed operation at low power levels, and with small signal swing and low noise margins, it was necessary to develop a hardware technology capable of meeting these needs. This is called 1A Technology hardware and is described in detail in another B.S.T.J. special issue.[3]

Since much of the circuitry in the No. 4 ESS peripheral area is composed of high-speed digital logic gates which are similar to the 1A Processor circuitry, it was decided that the No. 4 ESS equipment also would use the 1A Technology hardware to the greatest extent possible consistent with the requirement of the peripheral area. This permitted increased economies in manufacture due to greater quantities of similar

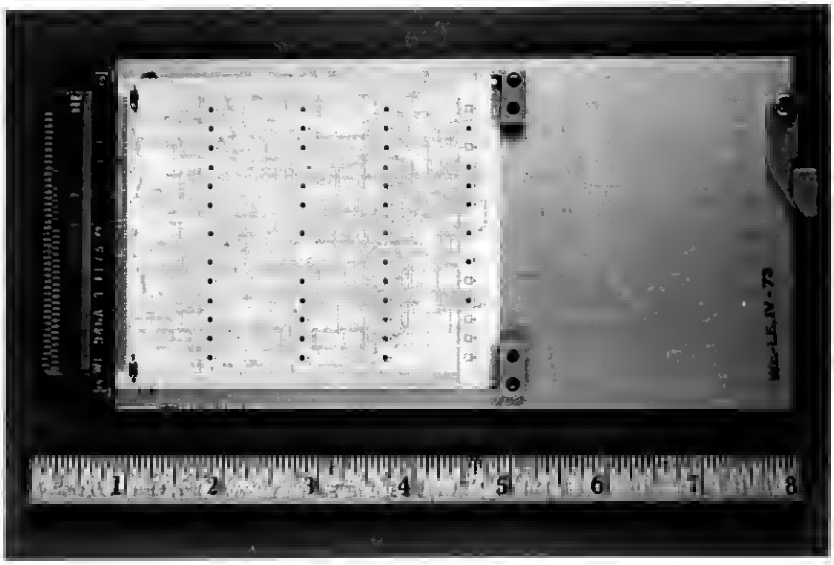

Fig. 14—Logic circuit pack.

items of manufacture, and it was not necessary to develop, design, and maintain two similar but different hardware systems.

Stated briefly, the 1A Technology hardware system is based upon a family of Collector Diffusion Isolation (CDI) chips. These CDI chips are all identical in external dimensions (0.050 inch by 0.050 inch over the tips of the beam leads) with each chip having 28 beam lead contacts. The family of codes consists of six general purpose codes and seven with specific functions. Up to 52 of these SIC chips may be mounted upon a large (3¼ inches by 4 inches) ceramic substrate and chips are interconnected with thin-film conductors. The standard substrate has predetermined locations for 52 SICs and 841 locations for arrays, each containing up to seven beam crossovers to facilitate wiring. The substrate is mounted upon an aluminum plate (7.31 inches by 3.67 inches by 0.062 inch), which acts as a heat sink and is fastened to an 82-pin connector. The bulk of the No. 4 ESS peripheral area circuitry has been built on 149 different codes of this type of circuit pack (Fig. 14).

Discrete circuit packs also were developed to cover that circuitry which was made up of discrete components or of combinations of SICs and discrete components. These circuit packs are packaged on conventional 1/16-inch-thick epoxy glass double-sided wiring boards measuring 3.67 inches by 7 inches. Interconnections between sides are provided by plated-through holes. The SICs are accommodated on the discrete circuit packs by small Hybrid Integrated Circuits (HICs). A HIC consists of a small ceramic substrate which mounts one or more SICs along with its

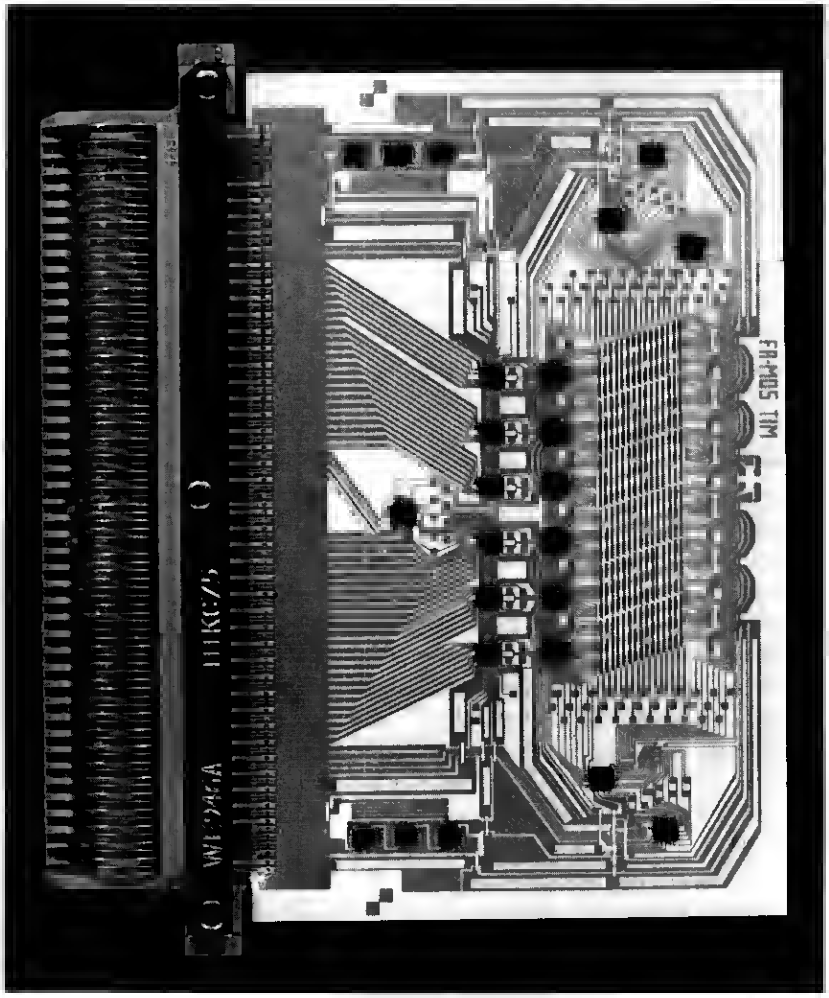

Fig. 15—Solid-state memory pack.

thin-film circuitry; in addition a HIC may contain thin-film resistors. The substrate then has a conventional lead frame added to it, which is used to mount the HIC to the epoxy glass board through holes in the board. Discrete components, which usually have axial leads, are mounted in the conventional fashion. The circuit pack can be equipped with either a 42-contact or an 82-contact plug connector. To date, 35 of those codes have been designed for use in the No. 4 ESS peripheral area.

As a special case, four solid-state memory packs have been developed to provide localized storage in the No. 4 ESS peripheral area. These circuit packs are organized as either 128- or 256-word by 10- or 12-bit arrays.

The memory function is provided by a silicon gate MOS chip which contains a 128-word by 2-bit array of static memory cells. Decoding, buffering, sensing, and digit driving are performed by bipolar chips. These chips are mounted upon a half-size ceramic substrate which is fastened to an aluminum heat sink and provided with a connector, as shown in Fig. 15.

The next level of assembly is the unit which is built up of a number of circuit packs assembled on a common mounting structure and interconnected at the backplane to perform one or more specific functions. Generally in a unit the circuit packs are located on ½-inch horizontal centers or multiples thereof and 4-inch vertical centers. Occasionally ¾-inch horizontal spacings are used.

Interconnections between the circuit-pack connector terminals in a given unit are accomplished by two methods. Multilayer boards are used for power and ground connections and for some signal connections. Most of the signal connections, however, are made with 30-gauge wire, which is machine-wrapped. Electrically sensitive leads are applied manually, generally as tight twisted pairs or miniature coaxial cables.

The final level of packaging is the frame, which consists of two or more units mounted upon a common structural framework. Intraframe wiring consists of twisted pair or miniature coaxial cables either loosely run via guides or in cable harnesses. Almost all of the interframe cabling is connectorized. All of the cables that carry telephone messages in the high-speed time domain are coaxial cables, while the rest are switchboard cable.

From the initial conception of the frame design to the acceptance tests at the central office level, thermal considerations were of the upmost importance. In the early designs, analytical studies using computer programs were made of the temperature rise within the frame under the maximum central office ambient temperature. The first models of the frames were tested at elevated temperatures in the hardware laboratory. As the System Laboratories were completed, the most heat-sensitive frames were tested in a system environment. Finally, major portions of the first two central offices were tested under operating conditions at elevated temperatures. All of these tests have confirmed the soundness of the original thermal design.

VII. SUMMARY

In this paper we have described the major items of the No. 4 ESS peripheral system, with particular emphasis on the switching network and the signaling interfaces. Much effort went into the planning and organization of these peripheral items to assure their compatibility with analog and digital transmission facilities and with existing and forward-looking signaling arrangements. To achieve this integration re-

quired the cooperation of many people in the transmission and switching organizations, as well as the gradual demolition of what once was a sacred boundary between the two disciplines.

REFERENCES

1. R. E. Staehler, "1A Processor: Organization and Objectives," B.S.T.J., special issue on 1A Processor, *56*, No. 2, pp. 119–134.
2. J. F. Boyle et al., "Transmission/Switching Interfaces and Toll Terminal Equipment for No. 4 E.S.S.," B.S.T.J., this issue, pp. 1057–1098.
3. J. O. Becker et al., "1A Processor: Technology and Physical Design," B.S.T.J., special issue on 1A Processor, *56*, No. 2, pp. 207–236.

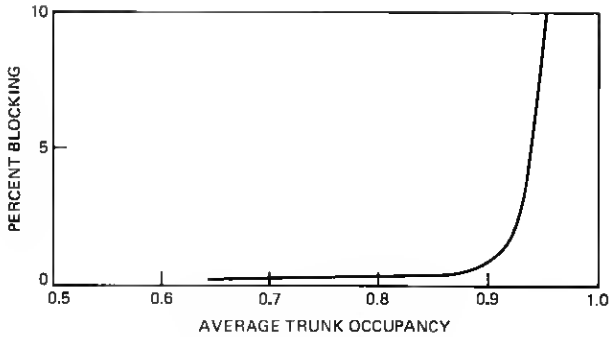

Fig. 3—No. 4 ESS network blocking.

represents the blocking curve of a full-size network. It shows the steep slope characteristic of highly efficient networks. The toll switching system requirements are:

0.5 percent blocking at 0.7 occupancy
10 percent blocking at 0.9 occupancy

The performance of the No. 4 ESS network is considerably better than these requirements.

Figure 4 shows the time (percentage of typical call setup time) used by the path-selection process. At high network occupancy, the usage amounts to about 10 percent. The efficiency of this process, as well as its stability at high loads, is an important factor in helping to achieve a very large call-handling capacity.

2.2 Topology

An initial decision was made to employ 1A Technology for all logic circuits in the time-division network. Based on the speed of these

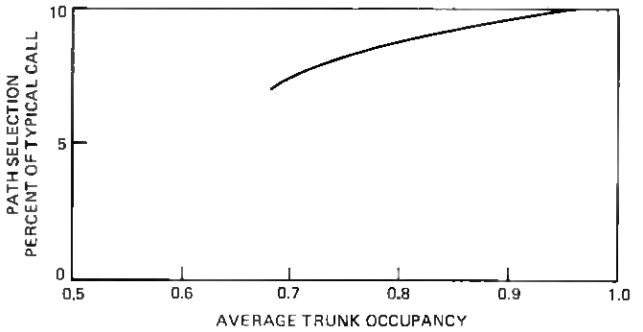

Fig. 4—No. 4 ESS network path-selection time.

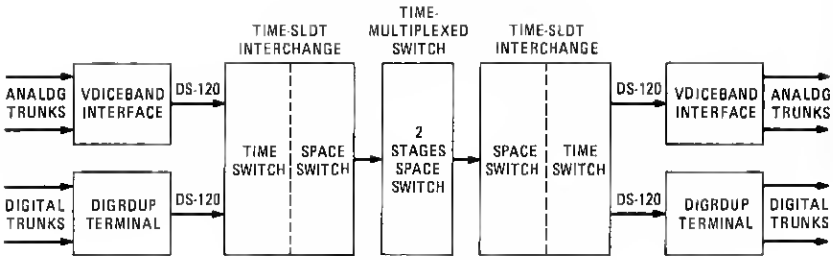

Fig. 5—No. 4 ESS time-division network topology.

semiconductor devices and on the characteristics of newly available solid-state memory units, another decision was made to operate the network at a rate of 128 time slots per PCM frame (125 μsec).

One of the early network topologies featured a combined concentrator, time switch and PCM codec. This was augmented with a three-stage space switch employing high-speed logic-gate switching elements. Such a network design, when concentrating 140 trunks on 128 time slots, was expected to be capable of handling about 72,000 trunks, each operating at 0.7 occupancy.

As development proceeded, the need for a still larger network was recognized. It was also decided to separate the PCM codec and time-switch functions to permit future digital signal processing (such as echo suppression) independent of switching. This led to the final network topology shown in Fig. 5. In this arrangement, the four-stage space-switch functions are distributed in two separate frame types—a time-multiplexed switch frame, and a time-slot interchange frame. The time-switch functions reside in the time-slot interchange frames, and the PCM functions are contained in a voiceband interface frame, which performs a purely sequential encoding of 120 trunks onto a fixed-format data link. This allows the PCM function to be located near the trunks, and provides a universal interface data link between transmission and switching frames—the DS-120 data link, which carries 120 trunks of PCM information on a 128 time-slot fixed-format signal. In addition, a direct digital switching interface is provided by digroup terminal units which multiplex five T1 digital carrier signals and connect (via a DS-120 link) to the switching frames in the same manner as the voiceband interface units. This network, at maximum size, can terminate 107,000 trunks and service circuits, each operating at 0.9 occupancy.

2.3 Description of switching network frames

2.3.1 Network clock frame

The network clock frame provides the basic timing and synchronization for the switching network. It generates a stable, accurate source